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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,984	11/25/2003	Mukta G. Faroog	END920030114US1	6936

23550 7590 12/16/2005

HOFFMAN WARNICK & D'ALESSANDRO, LLC
75 STATE STREET
14TH FL
ALBANY, NY 12207

EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/721,984	FAROOG ET AL.	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/25/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/721984 Attorney's Docket #: END920030114US1
Filing Date: 11/25/2003;

Applicant: Farooq et al.

Examiner: Alexander Williams

Applicant's election with traverse of species I, figure 2, claims 1-20, filed 10/27/05, has been acknowledged.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The use of the trademark Cupil-T has been noted in this application. It should be capitalized wherever it appears and be accompanied by the generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 to 20 are rejected under 35 U.S.C. § 102(b) as being anticipated by Shih et al. (U.S. Patent # 6,286,208 B1).

1. Shih et al. (figures 1 to 21) specifically figure 9 show a semiconductor module **59**, comprising: a semiconductor chip **30**; a substrate **65**; and an interposer structure **10** electrically connecting the semiconductor chip to the substrate, wherein the interposer structure includes metallurgical **22** through connections having a predetermined shape.

2. The semiconductor module of claim 1, Shih et al. show wherein the interpose member comprises an elastomeric, compliant material that includes the metallurgical through connections.

3. The semiconductor module of claim 1, Shih et al. show wherein the predetermined shape is selected from the group consisting of spherical, elongate, c-shaped, s-shaped and ellipsoid.

4. The semiconductor module of claim 1, Shih et al. further comprises support posts **56** positioned adjacent the interposer structure.

5. The semiconductor module of claim 4, Shih et al. show wherein the support posts **56** support a heat spreader **55** over the semiconductor chip.

6. The semiconductor module of claim 1, Shih et al. further comprising underfill **58** for sealing the interposer structure between the semiconductor chip and the substrate.

7. The semiconductor module of claim 1, Shih et al. show wherein the metallurgical **22** through connections of the interposer structure electrically connect an under bump metallization **32,24** of the semiconductor chip to a top surface metallization **63,64** of the substrate.

8. The semiconductor module of claim 7, Shih et al. show wherein the metallurgical through connections are soldered to at least one of the under bump metallization **32,24** or the top surface metallization **63,64**.

9. The semiconductor module of claim 1, Shih et al. show wherein the metallurgical **22** through connections are coated with gold.

10. Shih et al. (figures 1 to 21) specifically figure 9 show a semiconductor module **59**, comprising: a semiconductor chip **30** having an under bump metallization **32,24**; a substrate **65** having a top surface metallization **63,64**; and an interposer structure **10** electrically connecting the under bump metallization to the top surface metallization, wherein the interposer structure comprises an elastomeric, compliant material that includes metallurgical through connections having a predetermined shape.

11. The semiconductor module of claim 10, Shih et al. show wherein the predetermined shape is selected from the group consisting of spherical, elongate, c-shaped, s-shaped and ellipsoid.

12. The semiconductor module of claim 10, Shih et al. further comprises support posts **56** positioned adjacent the interposer structure for supporting a heat spreader **55** over the semiconductor chip.

13. The semiconductor module of claim 10, Shih et al. further comprising underfill **58** for sealing the interposer structure between the semiconductor chip and the substrate.

14. The semiconductor module of claim 10, Shih et al. show wherein the metallurgical through connections are soldered to at least one of the under bump metallization **32,24** or the top surface metallization **63,64**.

15. The semiconductor module of claim 10, Shih et al. show wherein the metallurgical **22** through connections are coated with gold.

16. Shih et al. (figures 1 to 21) specifically figure 9 show a method for forming a semiconductor module **59**, comprising: embedding metallurgical **22** through connections within an elastomeric, compliant material to form an interposer structure **10**; and positioning the interposer structure between a semiconductor chip **30** and a substrate **65** to electrically connect the semiconductor chip to the substrate.

17. The method of claim 16, Shih et al. show wherein the metallurgical **22** through connections electrically connect an under bump metallization **32,24** of the semiconductor chip to a top surface metallization **63,64** of the substrate.

18. The method of claim 17, Shih et al. further comprising soldering the interposer structure to at least one of the under bump metallization **32,24** or the top surface metallization **63,64**.

19. The method of claim 16, Shih et al. further comprising positioning support posts **56** adjacent the interposer structure to support a heat spreader **55** over the semiconductor chip.

20. The method of claim 16, Shih et al. further comprising sealing the interposer structure between the semiconductor chip and the substrate with underfill **58**.

(4) It is a constant endeavor to find ways of increasing the pinout density of integrated circuits (ICs). This is particularly important in ICs with high pin counts and relatively small packages. Solder ball connection (SBC) technology was developed to satisfy this growing need. In general the number of electronic circuits that can be manufactured per unit area of silicon or board space has increased dramatically in recent years. This increase in circuit density has produced a corresponding increase in the number of connections required between the various electronic circuits, integrated circuit modules, and boards to facilitate the manufacture of more complex products. High density integrated circuit modules such as microprocessors are typically housed in a protective package such as a pin grid array (PGA) module, that provides a means of connecting to other electronic circuits on a printed circuit board. PGA modules have an array of metal pins on the bottom side of the package. The

(5) PGA module is often connected and disconnected through these pins to a test card to evaluate the individual electronic circuit components before they are assembled into a final product. Connector sockets are available for PGA modules to facilitate the connection and disconnection of the PGA module for service, upgrade, or testing requirements.

8) U.S. Pat. No. 4,998,885, issued Mar. 12, 1991 to Beaman et al., is directed to an elastometer area array interposer. It provides for an elastomeric interposer surrounding fine metal wires which extend through the elastomeric materials permanently bonded to a rigid wiring substrate. It is useful for electrically connecting two substrates having high density interconnections. The structure described is comprised of conductive wires embedded in an elastomer material that are permanently bonded to the rigid wiring substrate. The contact interface is comprised of ball shaped gold wire conductors surrounded by an elastomer material. It is specifically adapted to interconnecting with flat gold plated pads on the surface of the mating substrate. The ball shaped contact surface is not large enough for use with an SBC type contact. SBC interconnection with this type of a ball shaped contact surface would cause excessive degradation of the connecting wires and ball shaped contact and limit the durability and reliability of the interface for socket applications.

(9) U.S. Pat. No. 5,371,654, issued Dec. 6, 1994 to Beaman et al., is directed to a structure for packaging electronic devices, such as semiconductor chips, in a three dimensional structure. The structure includes a multilayer wiring substrate for X-Y connections along with an elastomeric connector for Z axis connections. The elastomeric connector described is specifically adapted to a three dimensional packaging approach and does not require a contact interface with high durability. Also, the contact interface in this patent is comprised of an elastomeric connector having gold wire conductors mated to flat gold plated pads on the surface of the multilayer wiring substrate. The contact interface on the elastomeric connector would not be compatible for connection to the solder ball on an SBC module.

Claims 1 to 3, 6 to 8, 10, 11, 13, 14, 16 to 18 and 20 are rejected under 35 U.S.C. § 102(e) as being anticipated by Beaman et al. (U.S. Patent Application Publication # 2004/0135594 A1).

1. Beaman et al. (figures 1 and 2) specifically figure 2 show a semiconductor module, comprising: a semiconductor chip **1**; a substrate **2**; and an interposer structure **7** electrically connecting the semiconductor chip to the substrate, wherein the interposer structure includes metallurgical **18** through connections having a predetermined shape.

2. The semiconductor module of claim 1, Beaman et al. show wherein the interpose member comprises an elastomeric, compliant material that includes the metallurgical through connections.

3. The semiconductor module of claim 1, Beaman et al. show wherein the predetermined shape is selected from the group consisting of spherical, elongate, c-shaped, s-shaped and ellipsoid.

6. The semiconductor module of claim 1, Beaman et al. further comprising underfill **22** for sealing the interposer structure between the semiconductor chip and the substrate.

7. The semiconductor module of claim 1, Beaman et al. show wherein the metallurgical **18** through connections of the interposer structure electrically connect an under bump metallization **4** of the semiconductor chip to a top surface metallization **13** of the substrate.

8. The semiconductor module of claim 7, Beaman et al. show wherein the metallurgical **18** through connections are soldered to at least one of the under bump metallization **4** or the top surface metallization **13**.

10. Beaman et al. (figures 1 and 2) specifically figure 2 show a semiconductor module, comprising: a semiconductor chip **1** having an under bump metallization **4**; a substrate **2** having a top surface metallization **13**; and an interposer structure **7** electrically connecting the under bump metallization to the top surface metallization, wherein the interposer structure comprises an elastomeric, compliant material that includes metallurgical through connections having a predetermined shape.

11. The semiconductor module of claim 10, Beaman et al. show wherein the predetermined shape is selected from the group consisting of spherical, elongate, c-shaped, s-shaped and ellipsoid.

13. The semiconductor module of claim 10, Beaman et al. further comprising underfill **22** for sealing the interposer structure between the semiconductor chip and the substrate.

14. The semiconductor module of claim 10, Beaman et al. show wherein the metallurgical **18** through connections are soldered to at least one of the under bump **4** metallization or the top surface metallization **13**.

16. Beaman et al. (figures 1 and 2) specifically figure 2 show a method for forming a semiconductor module, comprising: embedding metallurgical **18** through connections within an elastomeric, compliant material to form an interposer structure **7**; and positioning the interposer structure between a semiconductor chip **1** and a substrate **2** to electrically connect the semiconductor chip to the substrate.

17. The method of claim 16, Beaman et al. show wherein the metallurgical **18** through connections electrically connect an under bump metallization **4** of the semiconductor chip to a top surface metallization **13**of the substrate.

18. The method of claim 17, Beaman et al. further comprising soldering the interposer structure to at least one of the under bump metallization **4** or the top surface metallization **13**.

20. The method of claim 16, Beaman et al. further comprising sealing the interposer structure between the semiconductor chip and the substrate with underfill **22**.

[0025] In FIG. 2 there is shown a schematic cross sectional view of the compliant interposer of the invention compressively positioned at the interface between the IC, element 1 and the fan out board, element 2, the input to the testing equipment.

[0026] Referring to FIG. 2 a compliant interposer 7 of the invention is positioned in a stack between the IC 1 and the board 2.

[0027] In the IC 1 the input-output contacts 4, of which an exemplary four are shown are shown, are positioned at the surface 3 of the IC 1 at the interface 8 with the compliant interposer 7.

[0028] In considering the stack in FIG. 2 made up of the IC element 1 at the interface 8 contacting the compliant interposer element 7 and in turn contacting the fan out input wiring board element 2; the interposer 7 structure includes external layers 9 and 10, each having a pattern of holes through the respective layer 9 and 10 in the configuration of the pads 4 on the adjacent surface 3 of the IC 1 and the configuration of the pads 13 on the surface 14 of the wiring board 2. The layers 9 and 10 are supported, in their spaced apart relationship enclosing an area 12, by a frame member 16, that maintains them at the separation distance 15. The interposer 7 further includes curved conductors 17 joining each of the pads 4 to the pads 13. The conductors 17 each passes through a pair of respective configuration pattern holes in the layers 9 and 10 and each has a bend or curved region 18 within the area 12.

[0029] The fan out substrate 2 provides a means of fanning out the wiring from the contacts 13 on the surface 14 to the equipment used in testing and burn in of the IC 1. The fan out substrate 2 can be made from various materials and constructions including single and multilayer ceramic with thick or thin film wiring, or epoxy glass laminate construction with high density copper wiring. The contacts 13 are usually flush with the surface 14 while the bond pads 4 on the IC 1 which usually are of aluminum are typically recessed sightly below a surface **passivation layer 22** on the surface 3 of the IC 1.

[0030] In the testing operation the IC element 1 and the board element 2 are compressed on the interposer 7 by opposing forces 19 and 20 that close any gaps at interfaces 8 and 21 and each conductor 17 can accommodate differences in the level of pads 4 and 13 by movement in the area 12 at the bend 18. The compliant interposer 7 is compressed between the fanout substrate 2 and the IC 1 with each end of each of the curved interconnect wires 17 making contact to it's respective pad 13. The interconnect wires 17 pass through the pattern of holes in the layers 9 and 10 which serve as alignment masks. The frame 16 maintains separation of the layers 9 and 10. The ends of the interconnect wires 17 under compression are free to adjust contact pressure through the bend 18 in the area 12 to provide compliance and accommodation of differences in pad level.

Claims 1 to 8, 10 to 14 and 16 to 20 are rejected under 35 U.S.C. § 102(e) as being anticipated by Brandorff et al. (U.S. Patent # 6,756,797 B2).

1. Brandorff et al. (figures 1 to 6) specifically figure 2 show a semiconductor module, comprising: a semiconductor chip **30**; a substrate **10**; and an interposer structure **20** electrically connecting the semiconductor chip to the substrate, wherein the interposer structure includes metallurgical **90** through connections having a predetermined shape.

2. The semiconductor module of claim 1, wherein the interpose member comprises an elastomeric, compliant material that includes the metallurgical through connections.

3. The semiconductor module of claim 1, Brandorff et al. show wherein the predetermined shape is selected from the group consisting of spherical, elongate, c-shaped, s-shaped and ellipsoid.

4. The semiconductor module of claim 1, Brandorff et al. further comprises support posts **40,45** positioned adjacent the interposer structure.

5. The semiconductor module of claim 4, Brandorff et al. show wherein the support posts support a heat spreader **50** over the semiconductor chip.

6. The semiconductor module of claim 1, Brandorff et al. further comprising underfill **25** for sealing the interposer structure between the semiconductor chip and the substrate.

7. The semiconductor module of claim 1, Brandorff et al. show wherein the metallurgical **90** through connections of the interposer structure electrically connect an under bump

metallization **185** of the semiconductor chip to a top surface metallization **185** of the substrate.

8. The semiconductor module of claim 7, Brandorff et al. show wherein the metallurgical **90** through connections are soldered to at least one of the under bump metallization **185** or the top surface metallization **185**.

10. Brandorff et al. (figures 1 to 6) specifically figure 2 show a semiconductor module, comprising: a semiconductor chip **30** having an under bump metallization **185**; a substrate **10** having a top surface metallization **185**; and an interposer structure **20** electrically connecting the under bump metallization to the top surface metallization, wherein the interposer structure comprises an elastomeric, compliant material that includes metallurgical **90** through connections having a predetermined shape.

11. The semiconductor module of claim 10, Brandorff et al. show wherein the predetermined shape is selected from the group consisting of spherical, elongate, c-shaped, s-shaped and ellipsoid.

12. The semiconductor module of claim 10, Brandorff et al. further comprises support posts **40,45** positioned adjacent the interposer structure for supporting a heat spreader **50** over the semiconductor chip.

13. The semiconductor module of claim 10, Brandorff et al. further comprising underfill **25** for sealing the interposer structure between the semiconductor chip and the substrate.

14. The semiconductor module of claim 10, Brandorff et al. show wherein the metallurgical **90** through connections are soldered to at least one of the under bump metallization **185** or the top surface metallization **185**.

16. Brandorff et al. (figures 1 to 6) specifically figure 2 show a method for forming a semiconductor module, comprising: embedding metallurgical **90** through connections within an elastomeric, compliant material to form an interposer structure **20**; and positioning the interposer structure between a semiconductor chip **30** and a substrate **10** to electrically connect the semiconductor chip to the substrate.

17. The method of claim 16, Brandorff et al. show wherein the metallurgical **90** through connections electrically connect an under bump metallization **185** of the semiconductor chip to a top surface metallization **185** of the substrate.
18. The method of claim 17, Brandorff et al. further comprising soldering the interposer structure to at least one of the under bump metallization **185** or the top surface metallization **185**.
19. The method of claim 16, Brandorff et al. further comprising positioning support posts **40,45** adjacent the interposer structure to support a heat spreader **50** over the semiconductor chip.
20. The method of claim 16, Brandorff et al. further comprising sealing the interposer structure between the semiconductor chip and the substrate with underfill **25**.

(16) In a first embodiment, there is disclosed a probe card assembly for testing integrated circuits comprising: a multi-layered dielectric plate interposed between a probe head and a printed circuit board, the printed circuit board having arrayed upon its surface a first plurality of electrical contacts arranged in a pattern, the dielectric plate having arrayed upon its surface a second plurality of electrical contacts arranged in a pattern substantially matching the first plurality of electrical contacts; a planarizing interposer interposed between the ceramic plate and the printed circuit board, the planarizing interposer having a pattern of holes matching the pattern of electrical contacts on the printed circuit board and the dielectric plate; a mounting ring clamped to the plate and the mounting ring attached to the printed circuit board; and a third plurality of compliant electrical connectors disposed within a multiplicity of the holes arrayed in a pattern upon the planarizing interposer, the electrical connectors making electrical contact with the first plurality of electrical contacts and the second plurality of electrical contacts.

Claims 9 and 15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Brandorff et al. (U.S. Patent # 6,756,797 B2) in view of Shih et al. (U.S. Patent # 6,286,208 B1).

Brandorff et al. show the features of the claimed invention as detailed above, but fail to explicitly show the metallurgical through connections are coated with gold.

Shih et al. is cited for showing an interconnector with contact pads having enhanced durability. Specifically, figures 1 to 21) specifically figure 9 show a semiconductor module **59**, comprising: a semiconductor chip **30**; a substrate **65**; and an interposer structure **10** electrically connecting the semiconductor chip to the substrate, wherein the interposer structure includes metallurgical **22** through connections having a predetermined shape, wherein the metallurgical **22** through connections are coated with gold between a semiconductor chip and a substrate; and on an interposer structure **7** for the purpose of providing an improved electrical connecting device.

Therefore, it would have been obvious to one of ordinary skill in the art to use Shih et al.'s gold plated interposer connecting structure to modify Brandorff et al.'s interposer connecting structure for the purpose of providing an improved electrical connecting device.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/712,713,713,717,720,704,710,675,773,774,778,734,737,738,780 324/754,758,757,765, 174/255,256,260,261 361/748,760,761,762,767,769,771 439/65,66,91	12/11/05
Other Documentation: foreign patents and literature in 257/712,713,713,717,720,704,710,675,773,774,778,734,737,738,780 324/754,758,757,765, 174/255,256,260,261 361/748,760,761,762,767,769,771 439/65,66,91	12/11/05
Electronic data base(s): U.S. Patents EAST	12/11/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
12/11/05